AMENDMENTS TO THE CLAIMS

Claims 1-120 (Cancelled)

121. A circuit for testing that is capable of creating any of a plurality of creatable component video test patterns, comprising:

a pattern selection register that is operable to store and provide a pattern selection value indicating a component video test pattern selected for creation among the plurality of creatable component video test patterns, wherein each of the plurality of creatable component video test patterns is, when created, a complete television video picture suitable for testing of digital television video processing equipment;

a pattern generation state machine that is operable to control a sequencing of a creation of the component video test pattern selected for creation by providing a plurality of clear and increment signals;

a memory component that is operable to provide a table output value based on the plurality of clear and increment signals and the pattern selection value, wherein the memory component includes:

a header table that stores:

a plurality of data samples that each include a unique data word; and

a sequence of data that includes a portion of a repeating horizontal blanking data sequence for horizontal blanking lines, and further includes a repeat field that indicates a number of repetitions for the repeating horizontal blanking sequence; and

an output register that is operable to create the component video test pattern selected for creation based on the table output value.

122. The circuit of Claim 121, wherein the plurality of creatable component video test patterns includes sixteen component video test patterns.

123. The circuit of Claim 121, further comprising:

a pattern change detector that is operable to assert a change pattern signal if the pattern selection value changes, wherein the pattern generation state machine resets if the change pattern signal is asserted.

124. The circuit of Claim 121, wherein each of the unique data words is a unique ten-bit data word.

125. The circuit of Claim 124, wherein each of the plurality of data samples is a forty-bit data sample.

126. The circuit of Claim 121, the circuit further comprising:

a built-in self test circuit that stores, for each of the plurality of creatable component video test patterns, a pre-calculated expected checksum, wherein the built-in self test circuit is operable to perform actions, including:

determining a checksum for the component video test pattern output by the output register; and

comparing the checksum with the pre-calculated expected checksum for the selected component video test pattern; and

a BIST result output pin that is arranged to provide a BIST result signal that indicates a result of the checksum comparison.

127. The circuit of Claim 126, wherein determining the checksum for the created component video test pattern is accomplished concurrently with displaying a picture based on the created component video test pattern.

128. The circuit of Claim 121, wherein the memory circuit further includes an equalizer pathological table.

129. The circuit of Claim 128, further comprising:

a plurality of logic gates that are operable to select one of two values associated with reading from the equalizer pathological table based on a line count value and the pattern selection value.

130. The circuit of Claim 121, wherein each table in the memory component is organized as a plurality of five-sample segments; each of the five-sample segments includes four 10-bit data samples, and further includes a repeat field having a repeat value that indicates how many times the four 10-bit data samples are to be repeated; for each of the plurality of data samples that each include a unique data word, the repeat field has a value of one; and wherein for each of the five-sample segments other than the plurality of samples that each include a unique data word, the repeat field has a value greater than ten.

131. The circuit of Claim 130, wherein the memory component further includes:

a line index table that stores values indicating a number of lines to transmit before switching to and from vertical blanking lines to active video lines.

132. The circuit of Claim 131, further comprising:

a line counter that is operable to track a number of lines transmitted, and to compare the number of lines transmitted against values in the line index table to determine when to switch to and from vertical blanking lines and active video lines;

a sample counter; and

a repeat counter, wherein the repeat counter is employed in control of the repeating of each of the four 10-bit data samples a number of times indicated by the repeat value.

133. A circuit for testing that is capable of creating any of a plurality of creatable video test patterns, comprising:

a pattern generation state machine that is operable to control a sequencing of a creation of a video test pattern selected for creation among the plurality of creatable video test pattern; and

a memory component that is operable to provide a table output value based on the control of the sequencing, wherein the memory component includes:

a header table that stores:

a plurality of data samples that each include a unique data word; and

a sequence of data that includes a portion of a repeating horizontal blanking data sequence for horizontal blanking lines, and further includes a repeat field that indicates a number of repetitions for the repeating horizontal blanking sequence.

134. The circuit of Claim 133, further comprising:

an output register that is operable to create the component video test pattern selected for creation based on the table output value.

135. The circuit of Claim 133, further comprising:

a pattern selection register that is operable to store and provide a pattern selection value, wherein the pattern selection value indicates which of the plurality of creatable video test patterns has been selected for creation.

136. The circuit of Claim 133, wherein each of the unique data words is a unique ten-bit data word.

137. The circuit of Claim 136, wherein each of the plurality of data samples is a forty-bit data sample.

138. A circuit for testing, comprising:

a pattern selection register that is operable to store and provide a pattern selection value indicating a component video test pattern selected for creation among a plurality of at least sixteen creatable video test patterns, wherein the circuit for testing is capable of creating any of the plurality of at least sixteen creatable component video test patterns upon selection; and wherein each of the plurality of at least sixteen creatable component video test patterns is, when created, a complete television video picture suitable for testing of digital television video processing equipment;

a pattern generation state machine that is operable to control a sequencing of a creation of the component video test pattern selected for creation by providing a plurality of clear and increment signals;

a memory component that is operable to provide a table output value based on the plurality of clear and increment signals and the pattern selection value, wherein the table output value is provided by tracking a location in a data sequence based on the clear and increment signals, and wherein the memory component includes:

a line index table that stores values indicating a number of lines to transmit before switching to and from vertical blanking lines to active video lines; and

a header table that stores:

a plurality of forty-bit data samples that each include a unique ten-bit data word; and

a sequence of data that includes a portion of a repeating horizontal blanking data sequence for the horizontal blanking lines, and further includes a repeat field that indicates a number of repetitions for the repeating horizontal blanking sequence;

a colour table;

a PLL pathological table; and

an equalizer pathological table;

a plurality of logic gates that are operable to select one of two values associated with reading from the equalizer pathological table based on a line count value and the pattern selection value;

an output register that is operable to create the component video test pattern selected for creation based on the table output value;

a built-in self test circuit that stores, for each of the plurality of at least sixteen creatable component video test patterns, a pre-calculated expected checksum, wherein the built-in self test circuit is operable to perform actions, including:

determining a checksum for the created component video test pattern output by the output register; and

comparing the checksum with the pre-calculated expected checksum for the selected component video test pattern; and

a BIST result output pin that is arranged to provide a BIST result signal that indicates a result of the checksum comparison.

139. The circuit of Claim 138, wherein each table in the memory component is organized as a plurality of five-sample segments; each of the five-sample segments includes four 10-bit data samples, and further includes a ten-bit repeat field including a repeat value that indicates how many times the four 10-bit data samples are to be repeated; for each of the plurality of data samples that each include a unique data word, the repeat field has a value of one; and wherein for each of the five-sample segments other than the plurality of samples that each include a unique data word, the repeat field has a value greater than ten.

140. The circuit of Claim 139, further comprising:

a line counter that is operable to track a number of lines transmitted, and to compare the number of lines transmitted against values in the line index table to determine when to switch to and from vertical blanking lines and active video lines;

a sample counter; and

a repeat counter, wherein the repeat counter is employed in the control of the repeating of each of the four 10-bit data samples a number of times indicated by the repeat value.